

An Area Efficient Distributed Arithmetic Based DTT Using Approximated Circuit

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Abstract: *In recent years many works have been proposed to find a low power and area efficient hardware design of discrete cosine transform (DCT) algorithm. All these work aimed at reproducing the cost metrics of power and area while maintaining high speed and accuracy in DCT applications. But trigonometric functions are used and measure need to be taken to process this cosine values in digital systems. Here in this paper in order to reduce the number of arithmetic operations and replacing these trigonometric functions by polynomial based integer arithmetic DTT orthogonal transformation is proposed for low-complexity circuitry and low power consumption without compromising the quality. Here complex multipliers are replaced by shifter and adders for complexity reduction involved in matrix computations. Approximation error is less evenly distributed in non-trigonometric transform matrices. So here we introduce the approximate DTT with its associate fast algorithm to reduce the complexity. Finally hardware complexity and power reduction will be proved against DCT and its quality retention will also be proved through real time image processing applications.*

I. Introduction

In most of the existing frame recompression methods are designed independently of video encoder. Unfortunately, they did not intend to finely cooperate with encoder, but only focus on improving the compression ratio. Actually, many information can be used for frame recompression and make it work more efficiently with encoder. For example, IME, FME, and MC have different workload and bandwidth requirement, the precision of compression can also be different for each of them.

What is more, intra prediction in video encoder can be used to guide the recompression of each coding blocks. Frame recompression should take all of them into consideration, and make use of information from encoder. In this paper, an encoder friendly frame recompression scheme is proposed. This scheme fully uses the information from encoder and discriminate IME from FME and MC to finely save external memory bandwidth. There are two coding layer in our scheme: base layer (BL) and enhancement layer (EL). Base layer is lossy data which only used for IME.

Combining with enhancement layer, lossless data can be reconstructed and it is used for FME and MC. Base layer is compressed by proposed three new techniques: tailing-bit truncation (TBT), in-block prediction (IBP), and small-value optimized variable length coding (SVO-VLC).

Multimedia data processing, which encompasses almost every aspects of our daily life such as communication broad casting, data search, advertisement, video games, etc has become an integral part of our life style. The most significant part of multimedia systems is application involving image or video, which require computationally intensive data processing. Moreover, as the use of mobile device increases exponentially, there is growing demand for multimedia application to run on these portable devices.

II. Existing System

DCT algorithms with multiplier units are opted for high speed purpose but they tend to consume more power. Hence multiplierless Distributed Arithmetic based algorithms were proposed. In, a novel reconfigurable adder-based architecture for DA realizing the inner product which is the key computation in many digital signal processing applications was proposed. In ROM based DA architecture, the input signal correlations and quantization are exploited to reduce the arithmetic operation. The drawback of DA based architecture is that as the number of inputs and the internal precision increases, it needs a large size of ROM, which increases the hardware complexity. Several NEDA based algorithms which are free from ROM eliminates the redundancy in the conventional DA based DCT have been proposed.

1. The multiplier based discrete cosine transform were presented and implemented. It led into more complexity in hardware structure on application specific integrated circuit (ASIC) products in terms of fabrication and also increases in terms of truncation error.

2. Poor performance in terms of speed of multiplication process due to applied multiplier based DCT core on FPGA implementation.

III. Proposed System

DCT algorithm has diverse applications and is widely used for Image compression. Here we propose discrete Tchebichef transform (DTT) which is a non trigonometric fully polynomial-based orthogonal transform.

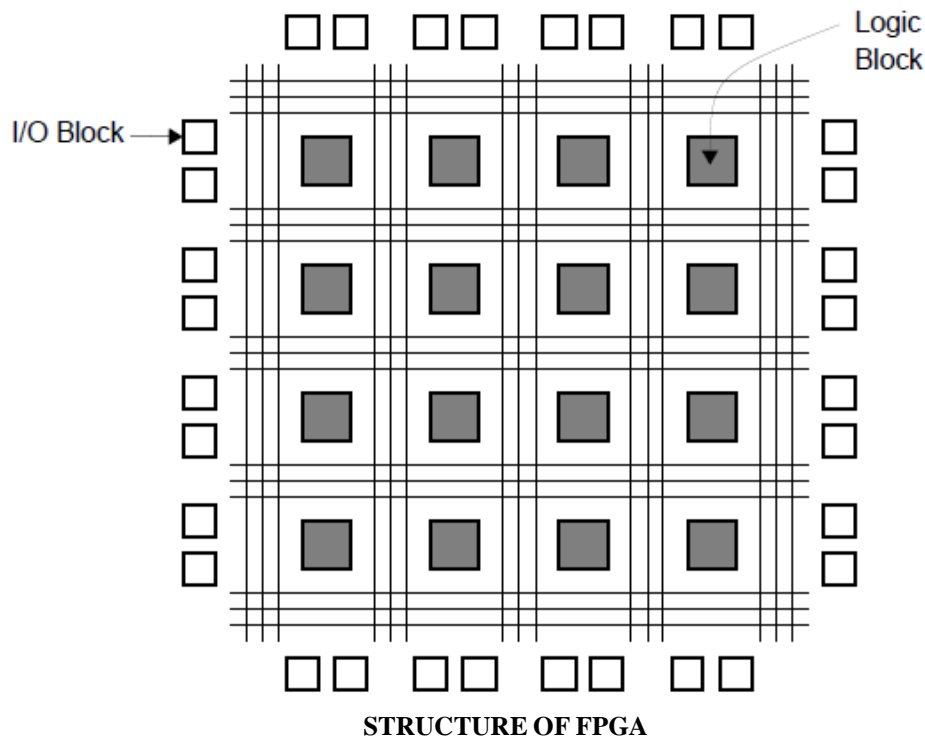
In terms of energy compaction and orthogonally DTT has similar properties as compared to DCT. Implementing DTT algorithm reduces the number of computations during processing, increases the accuracy of reconstruction of the image, and reduces the chip area of implementation of a processor built for this purpose. This reduces the overall power consumption.

Advantages

- Number of gates required in hardware implementation, such as on an FPGA, is minimum as hardware complexity is greatly reduced compared to other processors such as DSP multipliers
- It is relatively simple in design
- No multiplication and only addition, subtraction and bit-shifting operation ensures simple VLSI implementation.
- Delay involved during processing is comparable to that during the implementation of a division or square-rooting operation.

Either if there is an absence of a hardware multiplier (e.g. uC, uP) or there is a necessity to optimize the number of logic gates (e.g. FPGA) DTT is the preferred choice.

IV. Architecture Diagram



V. Conclusion

In this paper, we analyze the performance of DCT and DTT algorithm for prediction based video compression system. Initially we analyzes the DCT and its funtionlaity using MODELSIM. The proposed algorithm is based on MC to finely save external memory bandwidth. We also illustrated the performance of DTT algorithm in numerical simulations, and our algorithm shows a significant performance improvement compared to DCT, while the complexity is much lower compared to DCT based approach.

Future Work

The overall DTT efficiency is largely depends on accumulators(Adders) used for matrix computation. In order to propose the DTT architecture for real time applications here with SA (Speculative adder)adder and through computation of sum and carry overall efficiency will be increased..

References

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